Model 4818	ArchiTek FPGA Development Suite	for Talon Recorders

Features

- Complete development environment for **adding custom FPGA IP to Talon® recorders**
- Custom FPGA IP integration tutorials with example projects
- SystemFlow® recording software extension application examples
- Compatible with most Talon recorders
- Works together with Pentek's Navigator® Design Suite
- Works together with Xilinx's Vivado® Design Suite

Custom FPGA IP designs ...

- Allow recording of only critical data
- Reduce or eliminate post-processing requirements
- Reduce storage capacity requirements
- Reduce data offload time
- Provide additional record/play channels

Overview

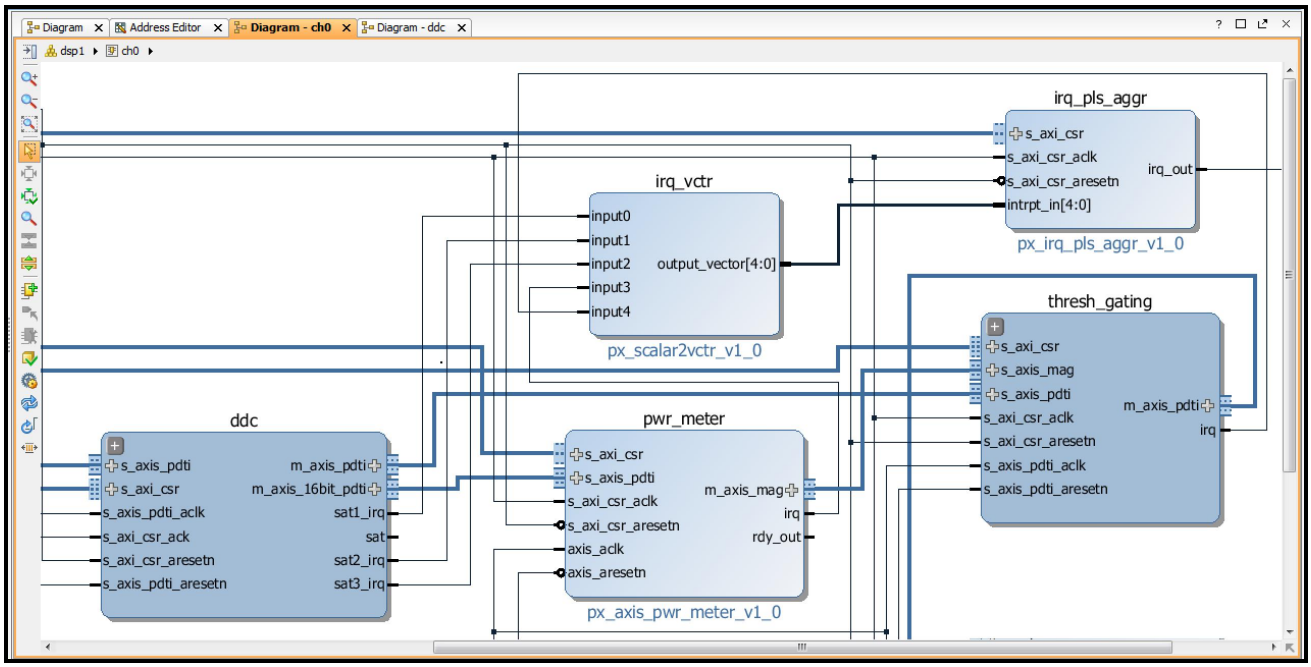
The ArchiTek™ FPGA Development Suite allows FPGA design engineers to add custom IP to a number of Pentek's Talon® recording systems. FPGA IP can be added to the recorder to provide real-time, on-the-fly digital signal processing during the data acquisition process, greatly reducing the time associated with post-processing recorded data. ArchiTek provides a simple development environment that allows engineers to add FPGA IP such as threshold detection, spectral filtering, digital downconversion, demodulation or any other digital signal processing technique required.

ArchiTek works together with Pentek's Navigator FPGA Development Kit (FDK) and Board Support Package (BSP) to provide a simple development environment that steps engineers through the process of integrating custom IP into the recorder. It includes SystemFlow API extensions and example projects that demonstrate custom FPGA IP integration along with modifications to the recording system's control interface.

ArchiTek also allows FPGA developers to add additional channels to the recording system, so users can record both processed and unprocessed data simultaneously. ArchiTek provides extensive documentation and tutorials to assist developers through the customization process, reducing risk along with development time.

ArchiTek Works in Conjunction with Navigator FDK

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater. The Xilinx Vivado Design Suite includes the IP Integrator, the industry's first plug-and-play IP integration design environment. Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek's Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

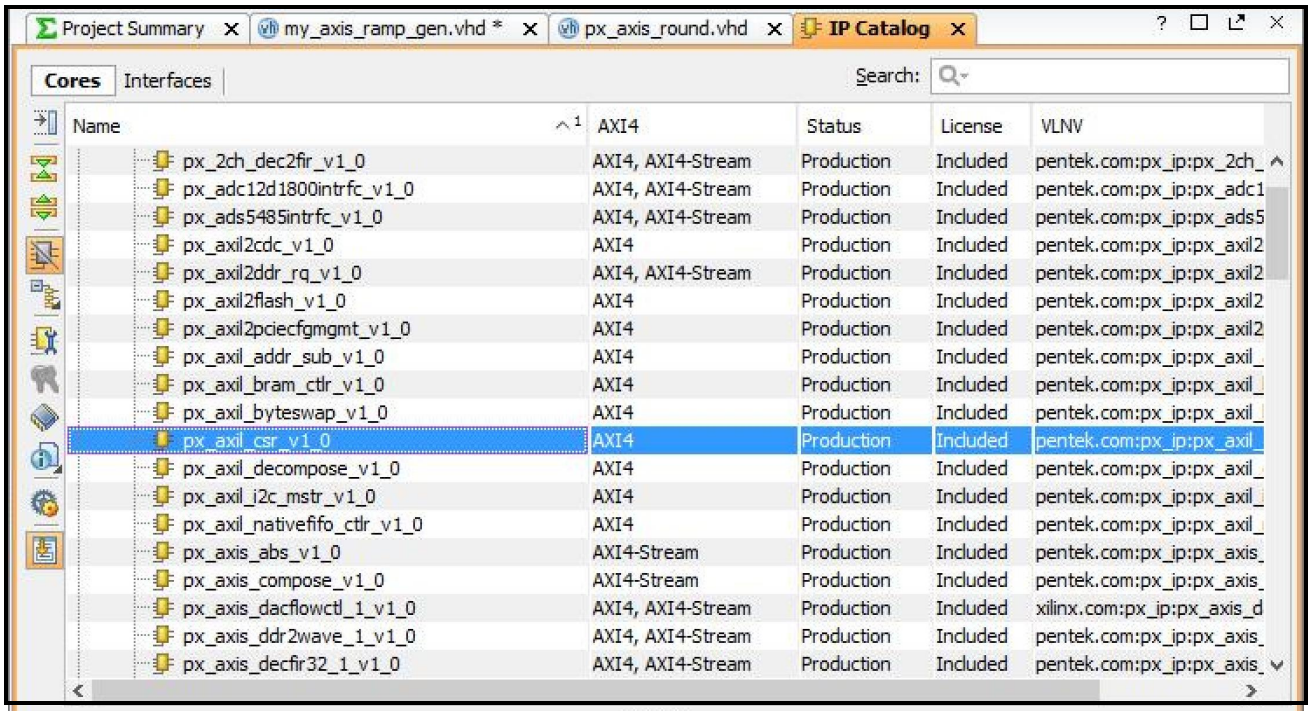


Pentek's Navigator FDK opened in Vivado's IP Integrator

Pentek's Talon recorders include boards that are shipped with a full complement of built-in IP based functions for data acquisition, waveform generation, data tagging and streaming, and processing to match the hardware features of the board. Each Navigator FDK provides the complete IP design for the board it supports. When the design is opened in Vivado's IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application. All blocks use industry standard AXI4 interfaces providing a well defined format for custom IP to connect to the rest of the design.

The Navigator FDK includes complete documentation, test benches and full VHDL source for developers who desire complete access to the IP.

NAVIGATOR
FPGA Design Kit



Navigator IP blocks are selectable from a pull-down list

In addition to the IP specific to an individual supported board, the Navigator IP core library also includes IP blocks for many common general purpose functions. These include processing blocks for some of the most commonly used algorithms. All IP blocks are easily accessible within the IP Integrator interface from a pull-down list.

ArchiTek Provides SystemFlow Enhancements

Every Talon recording system includes SystemFlow software. SystemFlow provides a graphical user interface (GUI) to control the recorder, signal analysis tools, and an API that allows users to integrate the Talon recorder into a larger system.

To support custom FPGA IP that is designed using the Navigator FDK, ArchiTek extends SystemFlow by providing generic commands for reading and writing control, and status registers to support custom IP blocks. During the IP creation process, FPGA registers are memory mapped and made available to the operating system. The API provides generic peek/poke style commands so users can read and write these custom developed registers. Developers can use these generic low-level commands to build higher level software libraries.

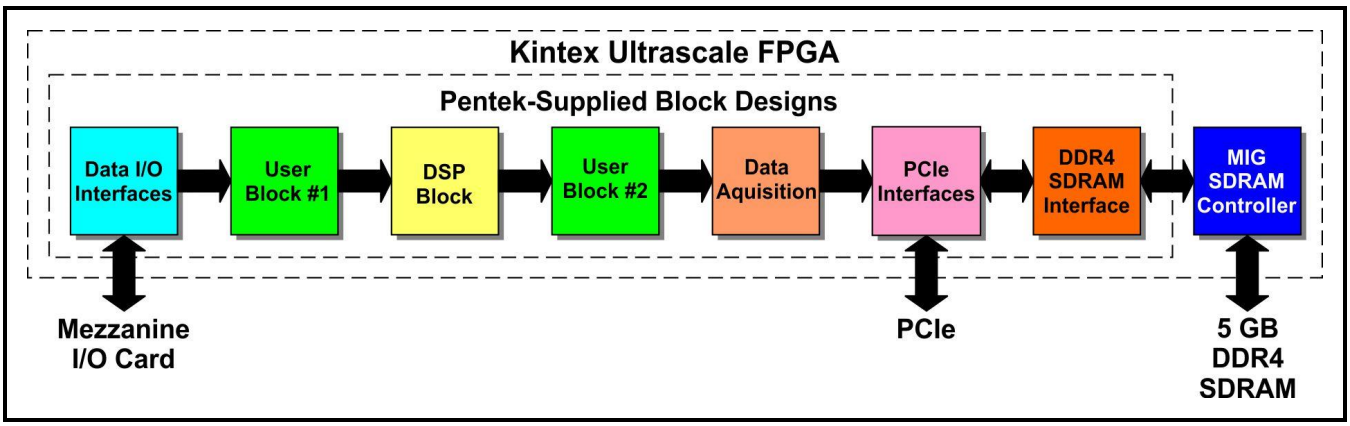
In addition to these low-level commands, SystemFlow supports the addition of DMA channels (record or playback channels) that are commonly required during FPGA customization. The Navigator FDK allows the user to add additional DMA channels by using Pentek-created DMA blocks, included as part of the FDK.

When adding new DMA channels, the FPGA memory map is structured to support the standard memory mapping convention defined by Pentek. This provides a simple mechanism for the SystemFlow software to "automatically" support new channels. ArchiTek documentation provides the steps required to add DMA channels, from simple modifications to the Navigator libraries to updates to the recorder's .ini file.

SystemFlow

Avoiding Custom IP Development Pitfalls

Developing custom IP for an FPGA requires an architecture that protects the user from breaking the existing IP and the corresponding recording software. The Navigator FDK provides user blocks at multiple locations in the data path to provide the user with some flexibility when performing data processing. The figure below provides a high-level example of the FPGA IP block diagram for Pentek's Jade Model 71861, which is used in a number of Talon recording systems.



Along with the Navigator FDK, ArchiTek provides the foundation and example projects for adding IP to user blocks and creating additional data path branches from an existing data streams. The structured design protects custom IP developers from breaking the recorder's standard functionality, reducing development time and risk.

Example Projects

ArchiTek provides example projects for the Navigator FDK and the SystemFlow API to demonstrate basic control of IP generated within a user block. These projects include FPGA source code, updated .mcs files and control software that is integrated into the SystemFlow recording software package to demonstrate the custom IP functionality. Other example projects include the addition of DMA (record/-play) channels.

Pricing and Availability

To learn more about our products or to discuss your specific application please contact your local representative or Pentek directly:

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